Development of FPGA based Prototype for Solar Tracker System

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Abstract— **The research paper presents a development of a prototype applicable for solar tracking systems. The angular movement of the sun (with respect to the Earth) was sensed using a set of photo sensors (arranged in a semicircle manner), thereby producing the binary input to the Field Programmable Gate Array (FPGA) based stepper motor driver system. The prototype is useful for angular movement of the solar panel, in accordance with the input signal provided at the stepper motor driver system. Right from a minimum to the maximum of 180 degree angular movement of the sun was considered, and it was targeted to obtain cosine angle of the order of zero degree between the solar panel and the sun. Due to this, the panel would collect maximum of the solar energy, at the times of sunrise as well as sunset too.**

Keywords— **Cosine angle, Earth movement, FPGA, Photo sensor, Solar panel, Stepper motor**

I. Introduction

The research work outlined in this paper deals with a prototype development of the angular movement of the solar panel mounted on the stepper motor shaft. More of the solar energy in the form of light-rays would be collected in the photovoltaic cells mounted on solar panel, only when there is cosine angle of zero degree between the sun and the solar panel. So the research work has developed a prototype that keep track on the angular movement of the sun, and moves the solar panel angularly to achieve the cosine angle zero between the sun and solar panel. The present paper focuses on the hardwared implementation of a high performance Field Programmable Gate Array (FPGA) based algorithm developed using Very High Speed Integrated Circuit Hardware Description Language (VHDL).

The FPGAs meet critical timing and performance requirements with parallel processing and real-time control application performance, allowing greater system integration and lower development cost. The position of sun at any time is a function of azimuth and altitude angle values. Azimuth and altitude angle values are collected off line [1].

A research group [2] reports that, in motion control systems, stepper motors are widely used and the stepper motor driver was mainly implemented using a DSP (digital signal processor). The DSP based driver's exhibit good performance; they are reliable, precise, and responsive. However, when mass production is needed, FPGA based drivers are preferred. Nowadays, with the improvement of FPGA techniques, it is possible to perform various computations in the FPGA, so it can be used instead of the DSP in motor driver design. The paper presents an open loop driver based on the FPGA. The driver performs stable, precise control and is responsive.

In the present research work a focus was given on moving the solar panel from minimum (presale) to 180 degree angle with respect to the horizontal axis of the earth. For example, in the morning time the panel will be directed towards the East and collect more light energy from the sun. On the contrary during the sunset also, it collects sun light by moving the panel with maximum i.e. tending towards 180 degree. The position of the sun will be automatically sensed by using a set of photo detector sensors mounted in a semi-circle manner. The binary output from such arrangement will be generated in the one-hot coding manner, pertaining with the position of the sun. One-hot encoding uses one flip-flop for each state. For example if there are 8 states in logic then it will use 8 flip-flops. This type of encoding is fast because only one bit needed to check for each state [3]. As per the input provided to the FPGA based control system, it makes angular rotation of the solar panel using stepper motor drive. A Finite State Machine (FSM) source code was developed for generating the stepper motor sequence.

II. FSM Soft IP Core Design Flow

The Fig. 1 shows an FSM designed to drive the stepper motor and generate the necessary sequence required to drive the motor coils. It shows that, the FSM is under the category Mealy machine [4], in which the output generated by the next state decoder is the function of present state as well as input signal. The input values shown in the sate machine of Fig. 1 are encoded in the decimal equivalent of the 8-bit binary numbers. When a bit becomes logic '1', as moving from right to the left i.e. from Least Significant Bit (LSB) to Most SB, there is a next state transition taking place.

The Fig. 1 shows that, the reset state is state0. There are eight states from state0 through state7, each one generates a four bit binary signal; required to drive the stepper motor coils. The 50 KHz clock source was generated inside the top level VHDL entity; developed in this research work. At the rate of this trigger frequency the state transition takes place.

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```
when state0 => if position="00000001" then
                  state<=state1;
                  mtr_coil<= "0110"; -- 6
              elsif position="00000000" then
                  state<=state0;
                  mtr_coil<= "0101"; --5
              end if;
          end case;
```

The code lines states that, when solar panel control system receives "00000001", it means that the sun position is angularly inclined and therefore, it is the time that the solar panel should take the angular movement with the predefined angle. Due to this, the solar panel would collect more of the sun energy. The angular movement of the panel takes place, only when stepper motor shaft rotates through its 'step-angle'. The movement is possible when two coil's current is fixed and remaining two coils current is altered. This was done by FSM producing "0110", which is a next state output signal, as compared to the previous one, in which the coil data was "0101". On the contrary, if there is 'position' signal "00000000", it reveals that there is no angular movement taken by the sun yet, meaning thereby, there is no need of taking angular movement for the solar panel. The remaining states from state1 to state7 have been coded in the similar manner; only the different outputs and different state transition conditions have been considered.
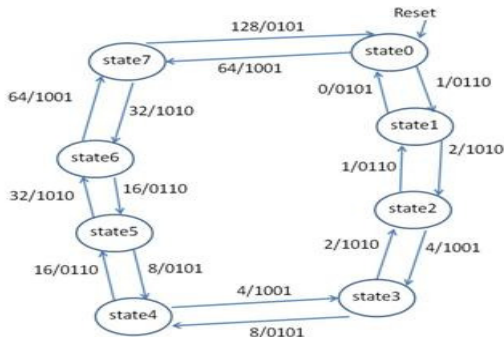

Figure 1.   Mealy FSM for Stepper Motor Sequence Generation.

III.   Synthesis result of the Soft IP Core

The Fig. 2 shows a Technology Schematic view of the synthesis result for the soft IP development obtained in Xilinx Integrated System Environment (ISE) design flow.

The device utilization summary of the soft IP core developed for solar tracking system is as shown in Table I. It mainly focuses on the percentage of FPGA resources available on the selected device from a family member, and produces the results of total utilization of the resources for the VHDL code. In this case the selected target device was Spartan 3E FPGA: xc3s500e-4fg320.

TABLE I.   INPUT SPEED DATA CAUSING THE DAC OUTPUT VOLTAGE CHANGE

| Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	41	9,312	1%
Number of 4 input LUTs	116	9,312	1%
Number of occupied Slices	78	4,656	1%
Number of Slices containing only related logic	78	78	100%
Number of Slices containing unrelated logic	0	78	0%
Total Number of 4 input LUTs	146	9,312	1%
Number used as logic	116		
Number used as a route-thru	30		
Number of bonded IOBs	14	232	6%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	2.82		
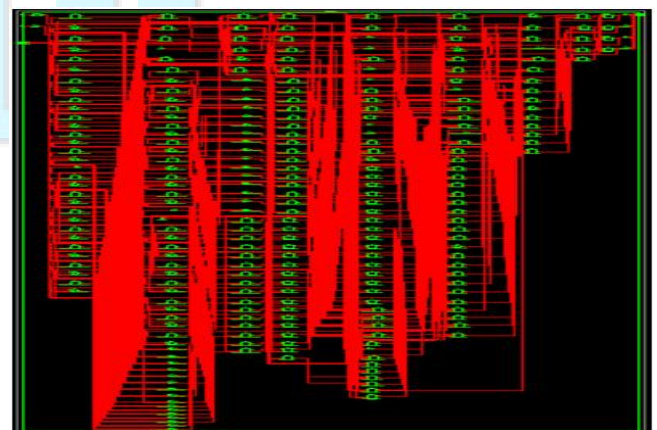
Figure 2.   Technology Schematic View of the Synthesis results for Soft IP Core

IV. Findings of the Solar Tracker Prototype Testing

As mentioned in the partial VHDL code lines, the solar tracker system accepts the position of the sun by means of the photo sensors mounted in a semicircle passion; thereby it produces a binary input for the FPGA core. At present there are 8 input lines taken for consideration, revealing the position of the sun moving angularly from minimum to 180 degree with respect to the horizontal axis of the Earth. In other words, if a LSB of the 8 bit input to FPGA core is asserted high, then it indicates that, the photo sensor associated with the least angular motion of the sun is taken place, meaning thereby, the input port of FPGA is "00000001". Then the FPGA generates a four bit vector signal in drives the stepper motor card generates the motor coil signals to rotate the solar panel with the one step angle.

The Fig. 3, shows the settings made at input (push button) switches available on the Nexys2 board developed by Digilent Inc. for Spartan 3E FPGA. For input signal named as 'position', the binary value was assigned to "00000000". As a result of process execution of the VHDL code, the Finite State Machine produces the four bit output signal "0101" at 'mtr_coil' signal.

Considering an angular movement of sun from minimum angle to the least step angle, the 'position' input "00000001"was applied to the FPGA system developed here. In response to this the motor coils signal was changed from "0101" to "0110", due to which the stepper motor moves with its single step angle and consequently the solar panel takes the same angular movement to collect more of the solar energy. This arrangement for producing a prototype input is shown in Fig. 4.

In the same way the stepper motor angular movement succeeded one step-angle ahead every time the successive bit asserted high. Importantly, when the position input was set to "10000000", as shown in Fig. 1, the state machine takes a state transition from state7 to state0, and therefore, the state0 related 'mtr_coil' signal was generated.
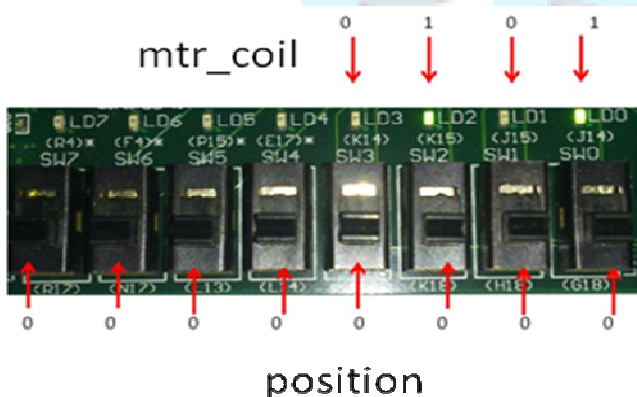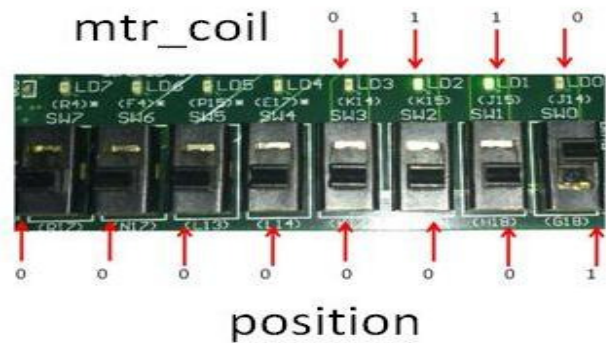

Figure 4. Input signal "00000001" to the FPGA core changes output signal from "0101" to "0110".

The Fig.5 illustrates the complete set of development comprising of an Digilent FPGA board: Nexys2, embedded with Spartan 3E device. The details of the Nexys2 board are given in reference manual [6]. It shows a motor driver card, consisting of four IC:ULN2003, current buffers required to drive the stepper motor coils; which are hunger of heavy currents itself. Seven buffers in each ULN2003 were connected in parallel to enhance the current capacity to seven times providing to each of the stepper motor coil. A stepper motor is also shown in Fig. 5 for testing purpose of the prototype for solar tracker. An 8 bit latch IC 74LS244 is also connected to accept and store the four bit coil related signal emerging from the FPGA board. The current requirement of the stepper motor depends upon the torque of the motor. The present stepper motor needs 1 A current for each of the coils. Therefore, a separate power supplying unit (Switch Mode Power Supply) being used in CPU cabinet of the computer was deployed here. A hard grounding was necessary between FPGA board and SMPS supply to run the stepper motor successfully.
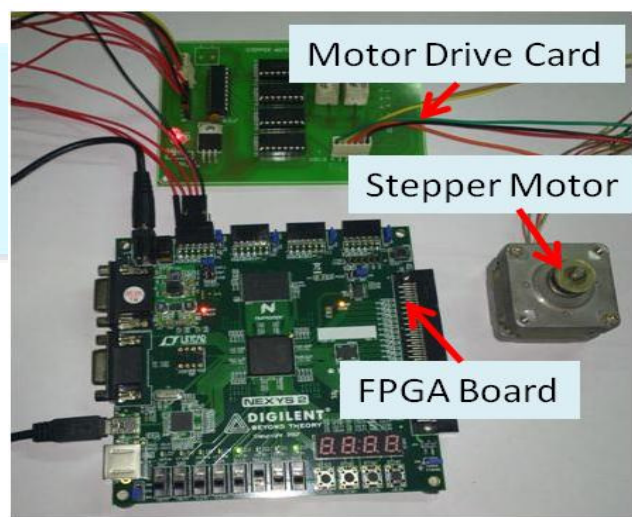

Figure 5. Prototype Development for Solar Tracker System comprising of FPGA board, Stepper Motor Driver Card and Stepper Motor.

Figure 3. Input signal "00000000" to the FPGA core produces "0101".

v. Conclusion and Future Scope

The system developed in this research work is a prototype for solar tracker system, which senses the angular position of the sun with respect to the Earth. The panel mounted on the stepper motor shaft was made to take an angular movement to obtain zero degree cosine angles between the pane and sun (with respect to the horizontal Earth axis), thereby collect more of the solar energy during sunrise as well as sunset.

In future, the system could be advanced using a relay, which activates the stepper motor driver card; only when there is pre defined angular movement of the sun take place. Due to such kind of triggering, the static current moving through the stepper motor coils would not flow unnecessarily for a long time. To increase the step-angle in future (for which the different step-angle motors needs to be selected), the number of photo sensors mounted in a semicircle manner are to increase.

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