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Design and Implementation of Low Power Multiternary Digit Adder

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Abstract

This paper presents an efficient multiternary digit (trit) adder design using decoder. Ternary logic is three valued logic represented by 0,1,2. The adder is based on an efficient single-trit full-adder design with low-complexity encoder and reduced complexity carry generation unit. The number of encoder and decoder blocks required while putting together several single-trit full-adder units to realize a multitrit adder. The ripple carry adder is designed using the ternary fulladder. Extensive simulation results shows the proposed multitrit adder design using decoder has low power and less area compared to the multi trit adder using multiplexer.

Index Terms—*Carbon nanotube field effect transistor (CNTFET), multiternary digit adder, power-delay product, ternary digit (Trit).*

I. INTRODUCTION

TECHNOLOGY scaling has been pursued aggressively during the last few decades to accommodate more transistors in the same chip. However, material properties are a function of the dimension. With respect to the classical Si-MOSFET, as the physical gate length is reduced to nanometers, the MOSFET exhibits short channel effects such as direct tunneling between source and drain and large parametric variations. These effects challenge further scaling of silicon devices. As a result, there has been tremendous interest in development of new structures and materials. New technologies include the carbon nanotube field effect transistor (CNTFET), single electron transistor, silicon-on-insulator, and fin-field effect transistor. Among these, CNTFET is promising in view of ballistic transport and low OFF-current properties enabling high-performance and low power design [1]–[6]. This letter presents efficient designs of 1) a single-ternary digit (trit) adder and 2) a multitrit adder in CNTFET. Ternary logic is specifically chosen for the design since it has an elegant association with CNTFET. In particular, CNTFETs provide the possibility of realizing two distinct threshold voltages merely by the use of different diameters of the carbon nanotube [7].Further, ternary logic achieves sim plicity and energy efficiency in digital design since it reduces the complexity of interconnects and chip area. For example, 14-bit binary addition can be done (roughly) by a nine-trit adder.

There are two main contributions of this letter. First, a new single-trit full-adder design is presented with reduced complexity encoder and carry-generation unit (in comparison to prior designs in [8] and [6]). Second, a multitrit adder design is presented with savings in the total number of encoder and decoder blocks (in comparison to a direct extension of a single-digit adder). As a result, the overall propagation delay and power of the proposed multidigit adder are less than that of a direct realization. CNTFETs can be fabricated with Ohmic or Schottky contacts resulting inMOSFET-type or Schottky-barrier-type operation [9], [10]. Historically, CNTFETs have been of the Schottkytype. This letter assumes the MOSFET-type operation to facilitate comparisons with the results in [6]. We have assumed $I_d - V_{ds}$ and $I_d - V_{gs}$ characteristics depicted in [11] (the *I–V* characteristics of the CNTFET are similar to that of the MOSFET). Simulations in HSPICE using the MOSFET-like CNTFET model of [11]–[13] and the parameters suggested in [14] reveal 79% reduction in power-delay product for the proposed three-trit adder and 88% reduction in powerdelay product for the proposed nine-trit adder over a direct realization.

II. PROPOSED SINGLE-TRIT ADDER

Dhande and Ingole [8] present the design of a ternary halfadder based on ternary gates and provide extensions to a one-trit full-adder. An enhancement to the ternary half-adder of [8] is presented in [6] with the advantage of speed-up. Our singledigit adder

solution is based on a small modification of the ternary decoder in [6]. This leads to a lower complexity halfadder as well as full-adder. We focus on the full-adder here since it constitutes the building block of the multidigit adder. The general structure of a one-trit adder with three ternary inputs A,B, and C_{in} and two ternary outputs C_{out} and Sum as shown in Fig. 1. It turns out that the encoder and carry-generation unit in Fig. 1 can be improved upon (when compared with prior designs in [8] and [6]). The proposed modification of the decoder (in [6]) is

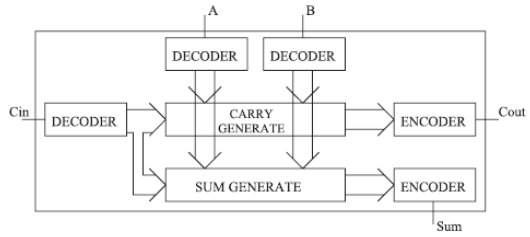


Figure1:Ternary full adder block Diagram

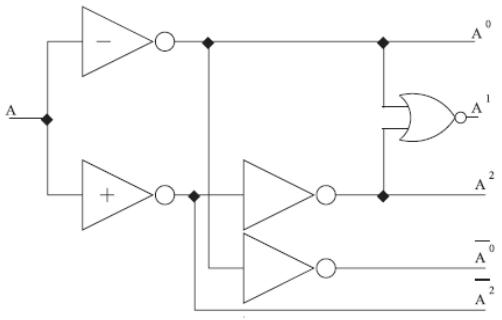
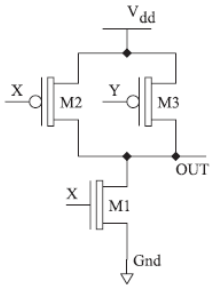


Figure 2:Decoder



X	Y	OUT	Voltage value
0	0	2	V_{dd}
0	2	2	V_{dd}
2	0	1	$V_{dd}/2$
2	2	0	0

Figure 3: Proposed Encoder

shown in Fig. 2. The ternary NOR gate of [6] is replaced here by a binary NOR since the inputs are Boolean. Also, complements of A_0 and A_2 are obtained with merely one inverter. While the circuit for *sum-generate* in Fig. 1 is the same as prior designs, the proposed *carry-generate* circuit requires fewer gates (as discussed later). Let the output carry of the *carry-generate* block in Fig. 1 when encoded (as 2 bits) be denoted by $C_{X\,o}$ and $C_{Y\,o}$ (these can be fed to the encoder of Fig. 3). Then, $C_{X\,o}$ and $C_{Y\,o}$ are given as: $C_{Xo} = \_(A,B,C_i) = (2,\ 2,\ 2)$. $C_{Yo} = \Pi(A,B,C_i) = \Pi\{(0,\ 0,\ 0),\ (0,\ 1,\ 0),\ (0,\ 2,\ 0),\ (1,\ 0,\ 0),\ (1,\ 1,\ 0),\ (2,\ 0,\ 0),\ (0,\ 0,\ 1),\ (0,\ 1,\ 1),\ (1,\ 0,\ 1),\ (0,\ 0,\ 2),\ (2,\ 2,\ 2)\}$. The simplified expressions for C_{Xo} and C_{Yo} are given by

$$C_{Xo} = A_2 + B_2 + C_2$$

$$C_{Yo} = (A_0 + B_2)(A_2 + B_0)(A_2 + C_{0i})(B_2 + C_{0i})(A_0 + B_0 + C_{0i})(A_0 + C_i)(B_0 + C_2)_i). \quad (1)$$

It is worth noting that C_{Xo} as well as C_{Yo} are independent of A_1 , B_1 , and C_{1i} . This has valuable consequences: the propagation to the next stage (especially for realizing a multitrit adder) becomes easier without *encoder–decoder* pairs (additional details are provided in Section III). Equation (1) suggests that the carries can be realized using only eight binary AND gates, one binary NAND gate, and one binary NOR gate. The availabil- ity of A_2 , B_2 , and $C_{2\ i}$ via the modified decoder (see Fig. 2) facilitates low-complexity carry generation.

TABLE I
REQUIRED DECODER OUTPUT FOR DIRECT PROPAGATION OF CARRY

Output	Encoder inputs		Actual outputs of Decoder			Required outputs of Decoder	
Z	E_1^X	E_0^X	D^2	D^1	D^0	D_0^Y	D_1^Y
0	2	2	0	0	2	2	2
1	2	0	0	2	0	2	0
2	0	0	2	0	0	0	0

Remark 1: A_0 output of the decoder is used in the derivation of equations of sum. The equations for sum are omitted since carry propagation is the key to multidigit adder design.

Remark 2: Dhande and Ingole [8] present a half-adder architecture that uses three ternary AND and one ternary OR (besides a T-buffer) for carry generation. The design in [6] realizes the carry using three binary AND and one binary OR (besides a T-buffer). The direct extension of the design in [6] to the fulladder requires 11 binary AND gates and 1 binary OR gate. With respect to the encoder in Fig. 1, the proposed design and its truth table are given in Fig. 3. Note that only three transistors are required here while a T-buffer followed by a ternary-OR gate are used in the design in [6]. Additional data in support of the savings are provided in Table II.

III. PROPOSED MULTITRIT ADDER IN CNTFET

Fig. 1 forms the basis for the design of an efficient multitrit adder. Consider the two-trit adder in Fig. 4 which is a direct extension of the one-trit adder of Fig. 1. In Fig. 4, the signal "X," which is two-digit valued has output carry information of first stage but in Boolean format. However, signal "Y," which is the decoded signal of first stage carry output is three-digit (three-valued). Therefore, signal "X" cannot be propagated to the next stage without conversion back to ternary. Since the encoder is simplified as shown in Fig. 3, if the decoder is designed to get "X" and

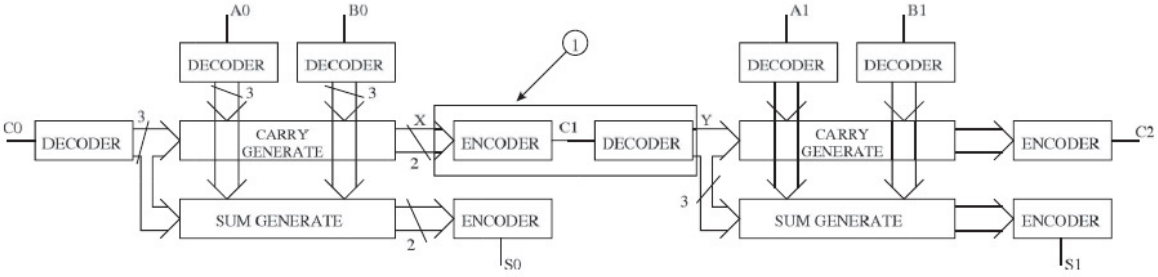


Figure 4:Two Trit Adder

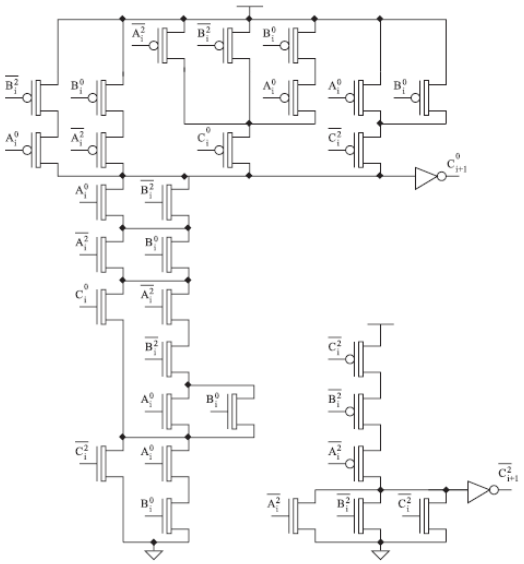


Fig. 5. Transistor-based realization of C0*i*+1 and *C*2*i*+1.

"Y" in Fig. 4 exactly the same, the block shown by _1 can be removed from the circuit leading to the reduction in overall propagation delay. To facilitate this, we construct Table I and study what is required by the decoder. It is clear from Table I that there are simple relations between the required decoder outputs and actual decoder outputs.

In particular, $D_2 = D_{Y0}$, $D_1 = \text{NOR}(D_{Y0}, D_{Y1})$, and $D_0 = D_{Y1}$.

Therefore, the actual decoder outputs can be evaluated directly from the encoder inputs without using the block shown by_1 in Fig. 4. Only "00" combination is considered as inputs of encoder for logic "2" output (instead of both "00" and "02" shown in Fig. 3) to avoid confusion with respect to the actual decoder outputs. The outputs at each stage, denoted by C_{2i} and C_{0i}, resemble the first stage carry C_{Xo} and C_{Yo} (see Section II). In particular, the output carry signals C_{2o} and C_{0o} become C_{21} and C_{01} for the first stage, C_{22} and C_{02} for the second stage and so on. Therefore, the carry signals of *i*th stage are given by (2). The circuit realizing these signals is shown in Fig. 5 $C_{2i+1} = A_{2i} + B_{2i} + C_{2i}C_{0i+1} = (A_{0i} + B_{2i})(A_{2i} + B_{0i})(A_{2i}B_{2i}(A_{0i} + B_{0i}) + C_{0i})(A_{0i}B_{0i} + C_{2i})$. (2)

The realization of a multitrit adder incorporating these ideas is given in Fig. 6. BLOCK A and BLOCK C are direct implementations of carry expressions and their duals, respectively, of a full adder whereas BLOCK B is for other unary signals (A_1, B_1, and C_{1i}) followed by the implementation of sum expressions of a full adder.

Remark 3: In the proposed encoder (see Fig. 3), there exists a path between V_{dd} and ground for an input combination of $\{X = 2, Y = 0\}$ leading to an output voltage of V_{dd} 2 and power consumption in standby mode due to static current (which becomes

significant for multitrit adders). This problem can be mitigated using power gating [15], [16].

TABLE II
COMPARISON OF SINGLE-DIGIT TERNARY FULL ADDERS

Adder type/ Parameter	Circuit of [6]	Proposed Ternary Adder
Worst-case Delay (τ) in ps	73.27	50.77
Average Power in μW	35.94	23.77
PDP in 10^{-15}J	1.72	0.85

In this approach, we connect an additional high-threshold voltage NMOS-CNTFET between ground and the source of the existing NMOS-CNTFET in the encoder (see Fig. 3). Enhancements can be obtained using the ideas in [15] and [16].

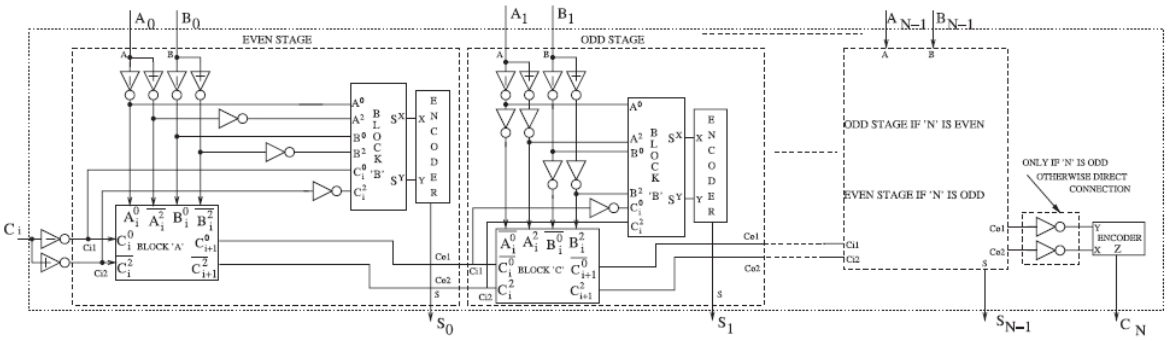


Figure6: Proposed Multi trit Adder

IV. SIMULATION RESULTS

In this section, we present the results of simulation using the MOSFET-like CNTFET model. The CNTFET model is described in detail in [11] and [13]. The simulation result of the proposed one-trit adder is shown in Fig. 7.

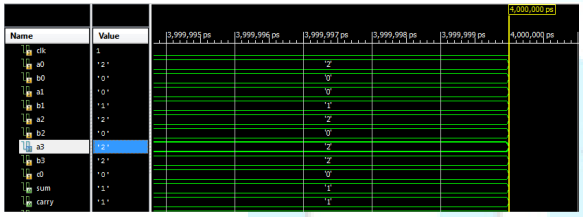


Figure 7: Transient response of multitrit adder

The propagation delays have been measured from change in input to possible transitions of sum and carry outputs. The simulation results are presented in Table II. The PDPis the product of average delay and average power consumption [6].

Table III presents the results for the proposed multitrit adders (and in particular for three-trit and nine-trit adders). Since no multitrit adders are available to our knowledge, we have also implemented a direct realization of three-trit and nine-trit adders based on the designs of the one-trit adder in [6].

Remark 4: We have so far assumed MOSFET-like CNTFET. Another type of CNTFET is the Schottky-barrier CNTFET (SB-CNTFET) that exhibits ambipolar nature [2], [7]. An ambipolar gate library has been recently proposed in [17].

TABLE III
COMPARISON OF THREE-TRIT ADDERS WITH EXISTING METHODS

Parameter/Adder Type	Power Delay Product(W)	Slice Fanout
Proposed half Adder	0.00032	19
Existing Half Adder	0.00035	23
Proposed Full Trit Adder	0.00039	50
Existing Full Trit Adder	0.00048	70

For SB CNTFET-based design, the approach in [17] provides savings

in transistors when binary logic is employed. Our ternarylogic approach (with enhancements to [6]) provides a design strategy applicable to different device structures.

V. CONCLUSION

New designs for single-trit and multitrit adders in CNTFET are presented. It is worth noting that the transistor-based design approach (as opposed to gate-level design) adopted for encoder as well as carry generation leads to an efficient solution. The proposed designs achieve low power-delay product.

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