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# CNTFET based 4-bit Carry Select Adder using Ternary Logic

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**Abstract**

The carbon nanotube field-effect transistor (CNTFET) is a promising device to supersede the MOSFET at the end of the technology roadmap of the CMOS. In all electronics applications adders are most widely used. Addition usually impacts the overall performance of the digital systems and crucial to arithmetic functions. Here the power dissipation is one of the important designs in all integrated circuits after the speed. In our paper presents the performance of the normal carry select adder and modified carry select adder which is modified by us. This comparison is done in three main performance parameters such as speed, area and power consumption. The results obtained from modified carry select adder better in area and power consumption and its speed is high. Here we are using CNTFET because it will show the operational characteristics due to gate capacitance and delay. In normal FET we will attain up to 20nm region. After that we cannot reduce this region. In our paper we are replacing BEC-1 (Binary to Excess1 Converter) instead of RCA (Ripple Carry Adder) in regular 16 bit CSLA (Carry Select Adder). BEC is designed by universal gates like NAND, NOR. Our paper is reducing the channel length in transistors by using CNT instead of silicon material. So our paper can reduce more number of logic Areas and Power consumptions.

***Keywords:*** *Adder, Carry Select Adder (CSLA), Ripple Carry Adder (RCA), Binary to Excess-1 Converter (BEC-1)*

## 1. Introduction

Design of power efficient high speed and area data path logic systems are one of the most substantial areas of research in VLSI system design. In normal

| Adder Blocks | Delay | Area |
|---|---|---|
| XOR | 3 | 5 |
| 2:1 Mux | 3 | 4 |
| Half Adder | 3 | 6 |
| Full Adder | 6 | 13 |

16 bit adders the speed is very slow. Because it has number of areas and its power consumption is very high. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next generation. The carry select adder (CSLA) is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However the carry select adder is not efficient in area because it uses multiple pairs of Ripple Carry Adder (RCA) to generate partial sum and carry in Cin=0 and Cin=1. Then final sum and carry selected for Multiplexer (Mux.). This paper replaces RCA by using BEC (Binary to Excess-1 Converter) and reducing the channel length in normal transistors and reducing Area and Power Consumption and increasing the speed.

## 2. Literature Survey

Ripple Carry Select Adder consist of cascaded "N" single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this transverses longest path called worst case delay path through N stages. Fig. 1 shows the block diagram of ripple carry adder. Now as the value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area. The basic idea of this work is to use Binary to Excess- 1 converter (BEC) instead of RCA with Cin=1 in conventional CSLA in order to reduce the area and power.

The BEC is designed by universal gates. Those gates have the transistors and its operations. In these transistors, the channel length is reducing by using CNT instead of channel material.

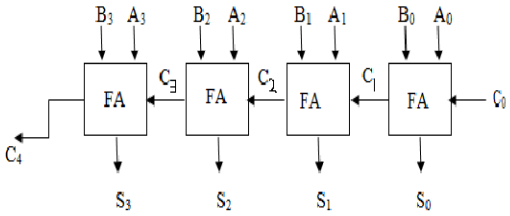


Fig.1 4-bit Ripple Carry Adder

## 3. Delay and Area Calculation of CSLA

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit.

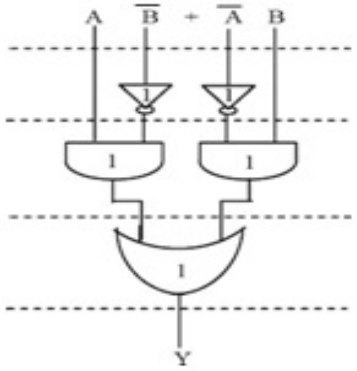


Fig. 2 Delay and Area evaluation of an XOR gate.

### 3.1 Basic Regular 16 bit Carry Select Adder

The structure of the 16-b regular CSLA is shown in Fig. 4.The delay and area evaluation of each group are shown in Fig. 3, in which the numerals within specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows.

1. The group2 has two sets of 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c1[time(t) = 7] of 6:3 mux is earlier than s3[t = 8] and later than s2[t = 6]. Thus, sum3[t = 11] is summation of s3 and mux[t = 3] and sum2[t = 10] is summation of c1 and mux.
2. Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows:
   fc6; sum[6 : 4]g = c3[t = 10] + mux
   fc10; sum[10 : 7]g = c6[t = 13] + mux
   fcout; sum[15 : 11]g = c10[t = 16] + mux:
3. The one set of 2-b RCA in group2 has 2 FA for Cin = 1 and the other set has 1 FA and 1 HA for Cin = 0. Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:
   Gate count = 57 (FA + HA + Mux)
   FA = 39(3 3 13)
   HA = 6(1 3 6)
   Mux = 12(3 3 4):
4. Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in Table 2.

| Group | Delay | Area |
|---|---|---|
| Group 2 | 11 | 57 |
| Group 3 | 13 | 87 |
| Group 4 | 16 | 117 |
| Group 5 | 19 | 147 |

Table 2: Delay and count of regulator CSLA groups

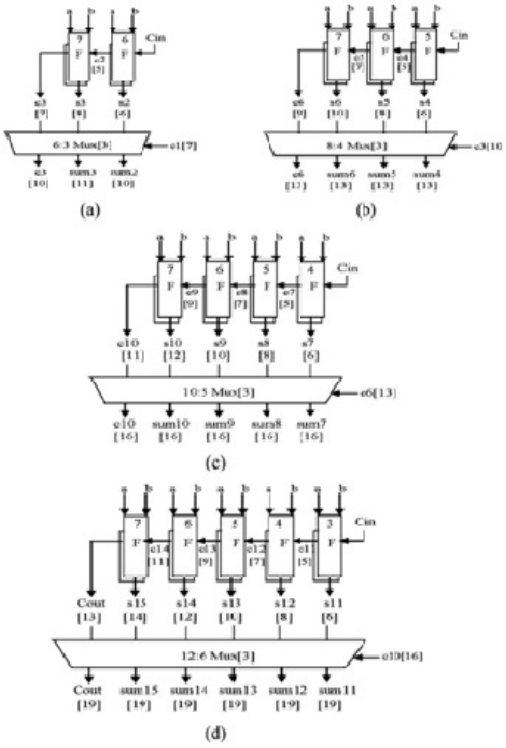


Fig. 3 Delay and area evaluation of regular CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. F is a Full Adder.

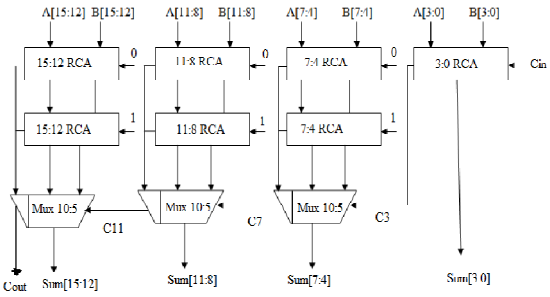


Fig. 4 Basic regular 16-b CSLA

## 3.2 Modified 16 bit Carry Select Adder

The structure of the proposed 16-b CSLA using BEC for RCA with Cin = 1 to optimize the area and power is shown in Fig. 6. The delay and area estimation of each group are shown in Fig. 5. The steps leading to the evaluation are given here.

1. The group2 has one 2-b RCA which has 1 FA and 1 HA for Cin = 0. Instead of another 2-b RCA with Cin = 1 a 3-b BEC is used which adds one to the output from 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c1[time(t) = 7] of 6:3 mux is earlier than the s3[t = 9] and c3[t = 10] and later than the s2[t = 4]. Thus, the sum3 and final c3 (output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.
2. For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.
3. The area count of group2 is determined as follows:
   Gate count = 43 (FA + HA + Mux + BEC)
   FA = 13(1 3 13)
   HA = 6(1 3 6)
   AND = 1
   NOT = 1
   XOR = 10(2 3 5)
   Mux = 12(3 3 4):
4. Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table IV. Comparing Tables III and IV,it is clear that the proposed modified SQRT CSLA saves 113 gate areas than the regular SQRT CSLA, with only 11 increases in gate delays. To further evaluate the performance, we have resorted to ASIC implementation and simulation.

Table 3: Delay and count of Modified CSLA groups

| Group | Delay | Area |
|---|---|---|
| Group 2 | 13 | 43 |
| Group 3 | 16 | 61 |
| Group 4 | 19 | 84 |
| Group 5 | 22 | 107 |

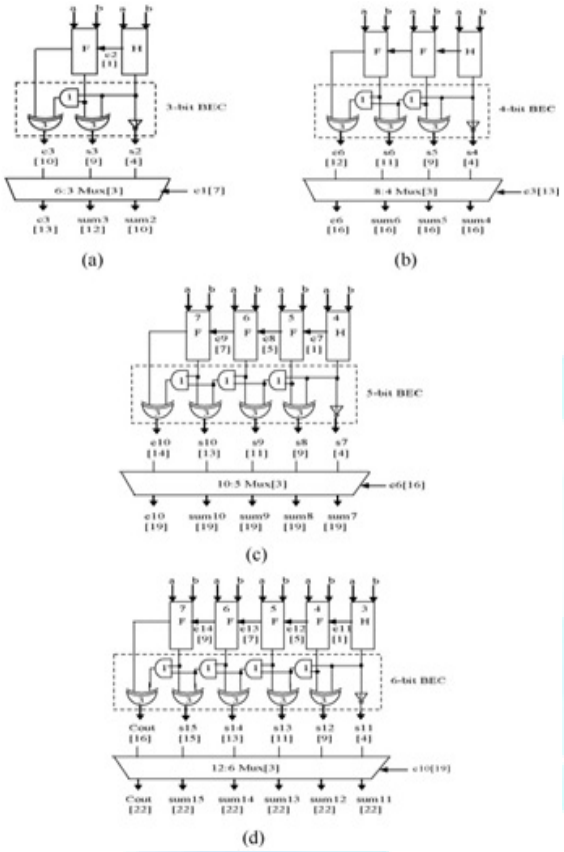


Fig. 5 Delay and area evaluation of modified CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. H is a Half Adder.

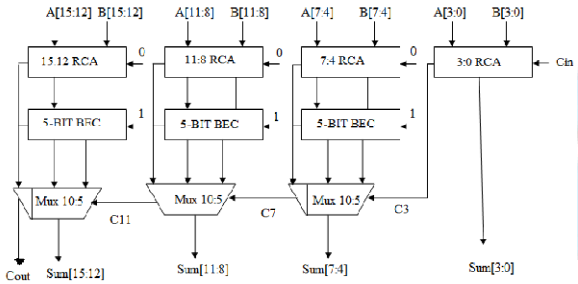


Fig. 6 Modified 16-b CSLA

## 3.3 BEC-1 (Binary to Excess-1 Converter)

As stated above the main idea of this work is to use BEC instead of the RCA with Cin = 1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n + 1-bit BEC is required. A structure of 4-b BEC is shown in Fig. 7.

Fig. 8 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols NOT, & AND;^XOR)

X0 = B0
X1 = B0^B1
X2 = B2^ (B0 & B1)
X3 = B3^ (B0 & B1 & B2)

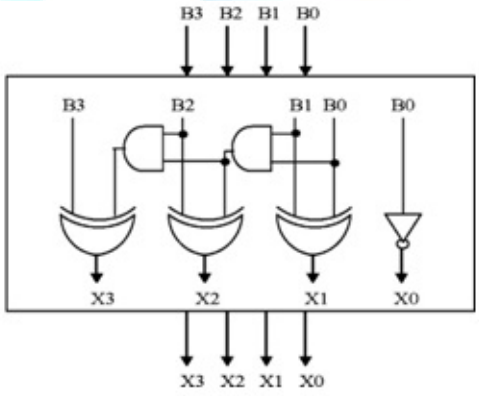


Fig. 7 4-bit BEC

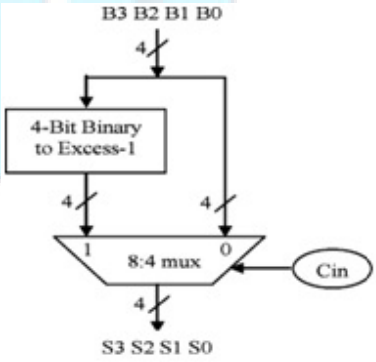


Fig. 8 4-bit BEC with 8:4 Mux

## 4. Ternary Logic

The ternary logic is sometimes equivalent to bivalent logic. The ternary logics gives 3 stages such as 1, 0 and intermediate values between 0 and 1. These three values is very important to calculate the characteristics of CNTFET. The 1's stage is ON condition stage and 0's stage is OFF condition stage.

## 5. CNTFET Structure and Model

The Carbon Nanotube Field Effect Transistor (CNTFET) is a promising device to supersede the MOSFET. It has advocated as one of the possible alternatives to replace the conventional MOSFET due to its performance characteristics. The electron movement in CNT is hopping so the mobility will be high in this CNTFET and automatically the speed will be increased due to mobility. In normal FET we can attain up to 20 nanometer region from some micro meter region. Further we can't able to reduce this region. If we reduce this region, a noise factor will be affected in electron movement path. So we are going for Moore's law. Moore's law is the number of transistors on integrated circuits doubles approximately every two years. So we are replacing alternate material for silicon is CNT. CNTs are sheets of grapheme rolled into tubes. The single walled CNT can be either metallic or semi conducting material. Semiconducting nanotubes have attracted the widespread attention of device.

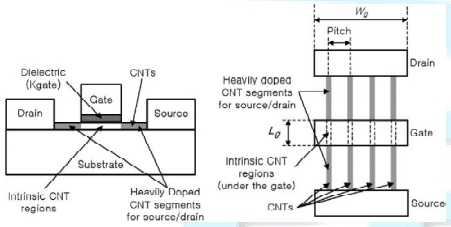


Fig. 9 CNTFET Structure

To evaluate the performance of a CNTFET, Various simulation models have been proposed and CNTFET HSPICE model is widely used in circuit design.

### 5.1 Gate Capacitance Model

The equation for the gate capacitance of a CNTFET is given in (1). The gate outer fringe capacitance to doped source/drain regions is ignored because outer capacitance is smaller than other components. When the gate height is 64 nm and the source/drain length is 32 nm.

$$Cgc = \min(N - NCD,\ 2) \times Cgc\_e + \max(N - NCD - 2,\ 0) \times Cgc\_m. \quad (1)$$

$$Cgc\_e = (Cgc\_inf \times Cgc\_sr) / (Cgc\_inf + Cgc\_sr) \quad (2)$$

$$Cgc\_m = 2Cgc\_e - Cgc\_inf = Cgc\_m\_symmetric. \quad (3)$$

Where,
Cgc –Gate to channel capacitance
N- Number of CNT
*Cgc_m*_symmetric is the capacitance for the case in which the pitch between the CNTs is constant
*N*CD- number of CNT undeposited

### 5.2 Drain Source current for CNTFET

$$I_{DS} = 2qkT/\pi h\ [f_0(U_{SF}/kT) - f_0(U_{DF}/kT)]$$

$$U_{SF} = EF - qV_{SC}$$

$$U_{DF} = EF - qV_{SC} - qV_{DS}$$

$$VSC = [-Qt + qNS(V_{SC}) + qND(V_{SC}) + qN_0]/C\Sigma$$

$$NS = 1/2 \int D(E)\ f(E - U_{SF})dE$$

$$ND = 1/2 \int D(E)\ f(E - U_{DF})dE$$

$$N0 = \int D(E)\ f(E - EF)dE$$

Where,
F0 represents the Fermi-Dirac integral of order 0.
K is Boltzmann's constant.
T is the temperature.
his reduced Planck's constant.
Qtrepresents the charge stored in terminal capacitances.
$V_{SC}$is the self-consistent.
D (E) is the density of states.
EF is the Fermi level; f is the Fermi probability distribution.
q is the electronic charge.
Erepresents the energy levels per nanotube unit length.
NS is the density of positive velocity states filled by the source, ND is the density of negative velocity states filled by the drain and $N_0$ is the equilibrium electron density.

## 5.3 Threshold Voltage for CNTFET

Table 4: $V_{TH}$ Calculation

| Cairal Vector | | Length | Minimum (Conduction Band) | Maximum (Valence band) | Eg (eV) | $V_{TH}$=Eg/2e |
|---|---|---|---|---|---|---|
| M | N | | | | | |
| 10 | 0 | 10 | -5.0 | 5.0 | 1.0 | 3.121*10^18 |
| 13 | 0 | 10 | -4.0 | 4.0 | 0.8 | 2.496*10^18 |
| 15 | 0 | 10 | -3.0 | 3.0 | 0.6 | 1.872*10^18 |
| 17 | 0 | 10 | -2.0 | 2.0 | 0.6 | 1.872*10^18 |
| 19 | 0 | 10 | -1.0 | 1.0 | 0.52 | 1.622*10^18 |

Here M and N are the cairal vectors or rotational vectors. In our project the silicon should be act as semiconductor. So the difference of the cairal vectors should not be zero and multiples of 3. If else the silicon will be act as conductor. If the minimum conduction band value and maximum valence band value is same value the silicon material act as conductor. The structure and electrical properties of the CNT is shown in figure.

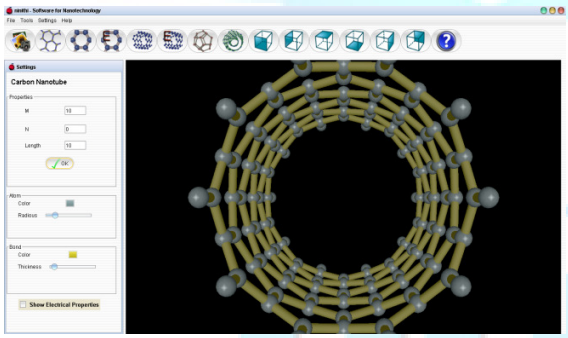

Fig. 10 Structure of CNT with M=10 and N=0

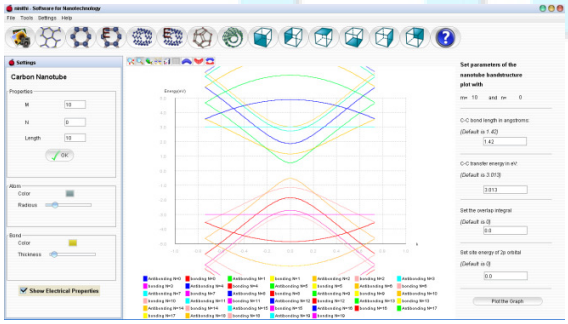

Fig. 11 Electrical properties of CNT with M=10 and N=0

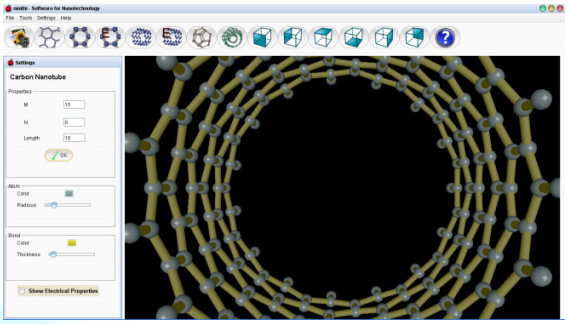

Fig. 12 Structure of CNT with M=15 and N=0

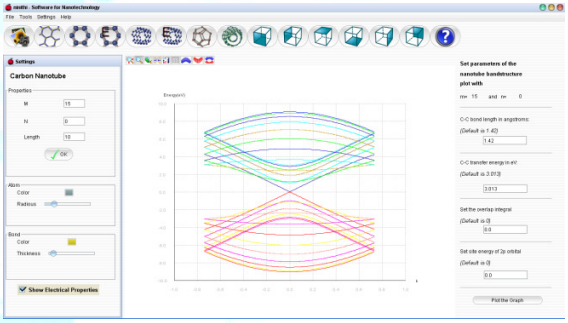

Fig. 13 Electrical properties of CNT with M=15 and N=0

## 5.4 Parameters of CNTFET

The important parameters of the CNTFET are thickness, dielectric constant, Nanotube diameter and temperature. The silicon is using here as channel material in transistor. So its dielectric constant is 3.9A, this dielectric material depends on the channel material. And have alternate material for silicon is High K Dielectric material. Here the thickness of the CNT is constant that is 1.5eV, temperature is room temperature (300K), and Length is 10 nm. These values have given by using mat lab coding and graph has plotted.

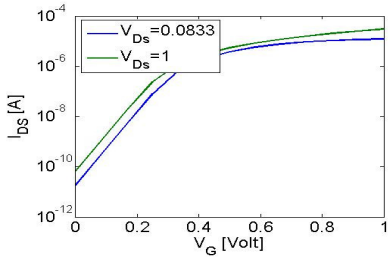


Fig. 14 $I_{DS}$Vs $V_G$

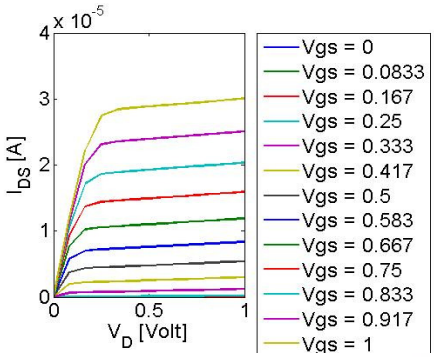


Fig. 15 $I_{DS}$Vs. $V_D$

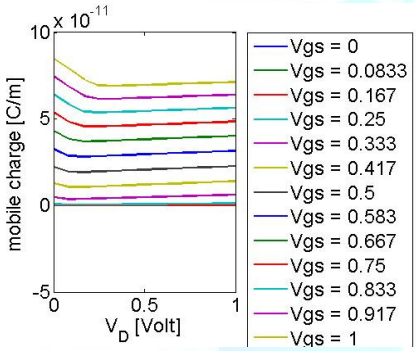


Fig. 16 Mobile charge vs. Drain voltage

## 6. Results

This work has been developed using Xilinx tool. The table 5 shoes the comparison between the various adders like regular CSLA and Modified CSLA and proposed CSLA for 8-bit, 16-bit, 32-bit and 64-bit. The parameters on which are compared are area, delay and power consumption. The fig. 17 depicts that the proposed CSLA has less number of gates and hence less area. Fig. 18 shows that the power consumption of proposed CSLA is reduced. It is clear that power, area of proposed CSLA is reduced.

Table 5: Comparison of Regular and Modified CSLA

| Word size | Adder | Area (no. of gate count) | Delay (ns) | Power (mW) |
|---|---|---|---|---|
| 8-bit | Regular CSLA | 200 | 14.46 | 94.48 |
| | Modified CSLA | 167 | 16.63 | 86.92 |
| 16-bit | Regular CSLA | 480 | 19.81 | 94.63 |
| | Modified CSLA | 381 | 21.59 | 81.38 |
| 32-bit | Regular CSLA | 1040 | 30.51 | 95.01 |
| | Modified CSLA | 809 | 32.65 | 79.81 |
| 64-bit | Regular CSLA | 2016 | 51.92 | 95.49 |
| | Modified CSLA | 1665 | 54.01 | 79.25 |

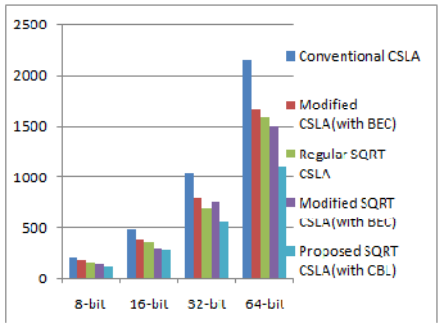


Fig. 17 Comparison of adders for area (no. of gate count)

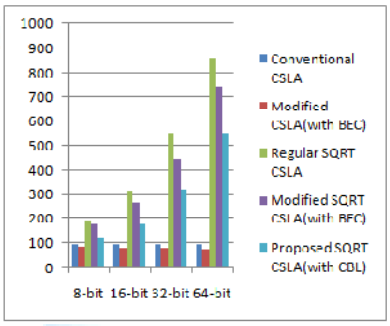


Fig. 18 Comparison of adders for power

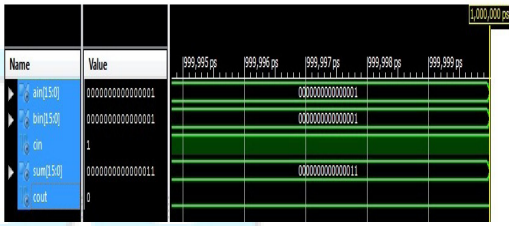


Fig. 19 Regular 16-bit CSLA

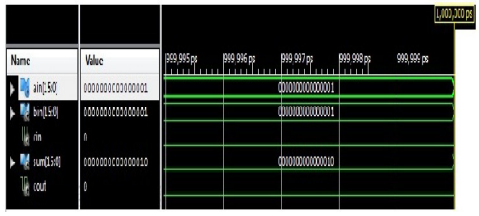


Fig. 20 Modified 16-bit CSLA

## 7. Conclusion

A simple approach is proposed in this paper to reduce the area and power of CSLA architecture. The reduced number of gates of this works using CNTFET and offers the great advantage in the reduction of area and also the total power. It requires less area and it is faster than ripple carry adder. The compared results show that the modified CSLA has a slightly larger delay. but the area and power of the 64-b modified CSLA are significantly reduced. The power-delay product and also the area-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere tradeoff of delay for power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. It would be interesting to test the design of the modified 128-b CSLA. It is mainly used in digital systems to perform fast arithmetic calculations and digital signal processers to execute FIR, IIR. This work may further extended by sharing common Boolean logic term and also by using AOI logic.

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