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Development of FPGA MicroBlaze Processor and GSM based Wireless Monitoring System for Neonatal Intensive Care Unit

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Abstract

In this research work a wireless embedded system is developed to monitor the physical parameters of Neonatal Intensive Care Unit (NICU). The system developed monitors the ambient temperature of the NICU using the temperature sensor and sends the information on the mobile phone in the form of Short Message Service (SMS). An Analogue to Digital Converter (ADC) was deployed to convert the analog output of the sensor into its corresponding digital equivalent. The Field Programmable Gate Array (FPGA) from Xilinx Inc. is the target device to implement a soft Intellectual Property (IP) core; necessary to monitor the temperature inside the NICU. By using Xilinx MicroBlaze Processor the Universal Asynchronous Receiver /Transmitter (UART) Soft IP Core was designed to send necessary Attention (AT) commands and drive the Global System for Mobile Communication GSM Module, SIM900A. The Core Generator tool from Xilinx ISE was used to design the MicroBlaze MCS embedded soft IP core and implemented on Xilinx Field Programmable Gate Array (FPGA) Spartan 3E device.

Keywords: *NICU, ADC, FPGA, Intellectual Property (IP), MicroBlaze soft processor core, UART, AT commands, GSM module, Core-Generator system.*

1. Introduction

The Neonatal Intensive Care Unit (NICU) is the technically advanced isolated room where the premature babies are kept under the continuous observation of neonatologist. It provides the environmental condition as its mother's belly. From the existing systems point of view, the Neonatal Intensive Care Units (NICUs) are facilitated with incubator along with the Radiant Warmer. An Incubator is a careful controller where the ambient temperature, humidity and skin temperature of baby can be maintained. It also helps to protect preterm infant from light, germs and noise that may cause infections, sickness or other types of diseases [1]. A Radiant Warmer is a body warming device maintaining the body temperature of the baby and limits the metabolism rate [2]. In case of baby incubators it is necessary to maintain the essential temperature around the baby. Usually the new born babies require warmer conditions as per their mother's womb. In case of premature babies the temperature should be maintained near about 34˚C to 37˚C [3].

In this research work the air temperature-probe LM35 was deployed to monitor the temperature around the baby. This sensor produces analogue electrical signal with respect to the temperature. The signal generated by LM35 is given to the serial Analogue to Digital converter 'PmodAD2', developed by Digilent Inc. The ADC generates 12 bit serial output proportional to the analogue voltage. This data information is transmitted towards the doctor's mobile phone through Global System for Mobile communication GSM module SIM900A using Universal Asynchronous Receiver Transmitter (UART) soft IP core of MicroBlaze processor. The soft IP core is generated in Very High Speed Integrated Circuit Hardware Description Language (VHDL) using Core Generator System.

The MicroBlaze embedded processor soft core is a reduced instruction set computer (RISC) optimized for implementation in Xilinx Field Programmable Gate Arrays. Xilinx's Embedded Development Kit (EDK) is the development package for building MicroBlaze embedded processor systems in Xilinx FPGAs [4]. This soft processor core is present in Core generator system. Xilinx CORE Generator System accelerates design time by providing access to highly parameterized Intellectual Properties (IP) for Xilinx FPGAs and is included in the Integrated Software Environment (ISE) Design Suite. CORE Generator provides a catalog of architecture specific, domain-specific (embedded, connectivity and

DSP), and market specific IP (Automotive, Consumer, Mil/Aero, Communications, Broadcast etc.). These user-customizable IP functions range in complexity from commonly used functions, such as memories and FIFOs, to system-level building blocks, such as filters and transforms. Using these IP blocks we can save days to months of design time [5].

The design flow for MicroBlaze embedded soft processor core is targeted for Spartan 3E FPGA board (Nexys2); developed by Digilent Inc. The reference manual of this board is given in [6].

The Xilinx Embedded Development Kit (EDK) is a collection of tools and Intellectual Properties (IP) that enables us to design a complete embedded processor system for implementation in a Xilinx FPGA device. EDK is designed to assist in all phases of the embedded design process. It provides the tools named as Xilinx Platform Studio (XPS) and Xilinx Software development Kit (SDK). XPS is used to design the hardware part of the embedded system and SDK is an integrated development environment, complementary to XPS, which is used for C/C++ embedded software application creation and verification [7].

2. Block Diagram of FPGA based Wireless Monitoring system for NICU

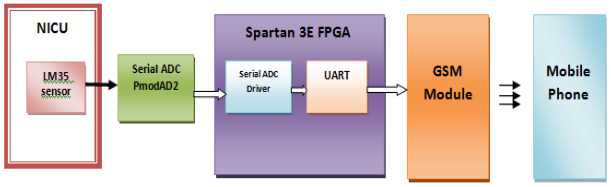

Fig.1 Block Diagram of FPGA based Wireless Monitoring system for NICU

The figure1 shows the block diagram of a wireless embedded system built around Spartan 3E FPGA device to monitor the ambient temperature of NICU.

The LM35 temperature sensor detects the temperature inside the NICU and produces the output in electrical form. This signal is fed to PmodAD2 serial analogue to digital converter. The IC7991 converts the signal into 12 bit digital equivalent. The AD7991 device operates on Inter IC communication protocol. For that, a soft IP module provided in [8] was implemented in the Xilinx FPGA Saprtan3E. The converted data was transmitted towards GSM module through UART IP core which was designed using MicroBlaze processor core. The reference manual of GSM SIM900A module is given in [9].

3. Designing of UART Soft IP Core Using MicroBlaze MCS Processor from Core Generator System.

The necessary steps to create MicroBlaze soft processor core based UART IP core for sending data information through GSM modem are discussed here. The MicroBlaze MCS core is present in Core generator system under the 'Embedded processing' tab of Architecture Wizard. As the on-board clock frequency of Spartan 3E Nexys2 board is of the order of 50 MHz, the input clock frequency for the MicroBlaze processor was also set to 50MHz. The memory size for the processor was selected to 16KB. The General purpose input (GPI) port and the General Purpose output (GPO) port of the processor were set to 8-bit.

Under the UART tab the Transmitter and Receiver were enabled and the baud rate was set to 9600. The figure 2 shows the MicroBlaze processor core, which was generated after clicking the 'Generate' tab. The core appears with the selected I/O lines, UART_Tx and UART_Rx lines along with Clock and Reset signals. The generated core was shown as .xco file in the hierarchy pane of the main ISE project.

A new top level entity with connections to the clock and peripherals on the Nexys2 board was created in Very High Speed Integrated Circuit Hardware Description Language (VHDL) by using the instantiation template generated by the Core Generator tool. The source code for the top level module was developed as shown below.

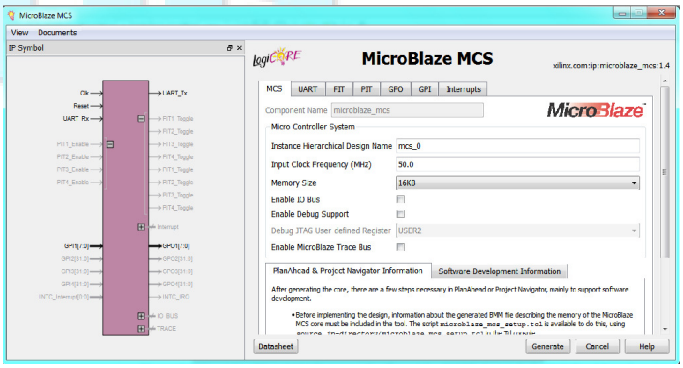

Fig.2 MicroBlaze MCS Processor Configured as UART

entity nicucode is

```
 PORT (
    Clk : IN STD_LOGIC;
    Reset : IN STD_LOGIC;
    UART_Rx : IN STD_LOGIC;
    UART_Tx : OUT STD_LOGIC;
    GPO1 : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
    GPI1 : IN STD_LOGIC_VECTOR(7 DOWNTO 0)  );
end nicucode;

architecture Behavioral of nicucode is

COMPONENT microblaze_mcs
  PORT (
    Clk : IN STD_LOGIC;
    Reset : IN STD_LOGIC;
    UART_Rx : IN STD_LOGIC;
    UART_Tx : OUT STD_LOGIC;
    GPO1 : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
    GPI1 : IN STD_LOGIC_VECTOR(7 DOWNTO 0));
END COMPONENT;

begin
mcs_0:microblaze_mcs
  PORT MAP (
    Clk => Clk,
    Reset => Reset,
    UART_Rx => UART_Rx,
    UART_Tx => UART_Tx,
    GPO1 => GPO1,
    GPI1 => GPI1);

end Behavioral;
```

Figure3 shows the Register Transfer Level (RTL) synthesis view of the top level module 'nicucode'. It gives the Xilinx ISE Design flow along with the hierarchy level of the Soft IP Core and the user constraint file (.ucf) created to interconnect necessary FPGA I/O lines with the top level entity.

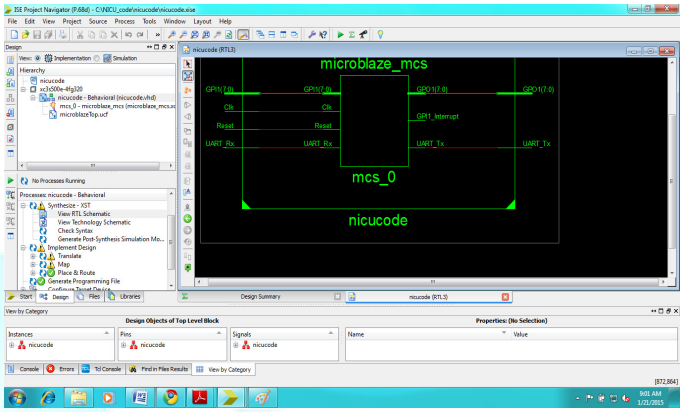

Fig.3 RTL Synthesis View of the Top Level Entity

The Figure 3 also illustrates 'microblaze_mcs' component interconnected with the 'nicucode' VHDL entity with an 8 bit input vector GPI (7:0), a clock input 'Clk' and 'Reset' input. To perform UART operation, and receiving the serial bits, another input port named as 'UART_Rx' is also shown. On the other side of the module, an output port 'UART_Tx' is shown, which transmits the serial bits towards the GSM module. The 8 lines of top level module were given to the LEDs available on the Nexys2 Spartan 3E board. These output lines are indicated as GPO (7:0).

4. Interfacing of GSM Module with UART Soft IP Core of MicroBlaze MCS Processor.

To Figure 4 shows the connection between Microprocessor based UART implemented on FPGA Spartan 3E device and GSM module SIM900A through a voltage converter IC 232 provided on the Nexys2 board as well as GSM module.

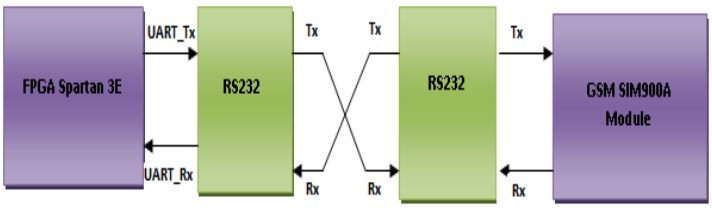

Fig.4 Interfacing of Microprocessor based UART and GSM SIM900A Module

From the figure it is clear that the UART_Tx from UART soft IP core was connected with the Rx terminal and

UART_Rx connected to the Tx line of GSM module. The necessary AT commands were sent from FPGA MicroBlaze Processor based UART to drive the GSM SIM900A module. Initially, these commands were monitored and tested on the Hyper Terminal of the Personal Computer.

Figure 5 shows the screenshot of the Hyper terminal window displaying the AT commands sent from FPGA Microprocessor based UART towards GSM module.

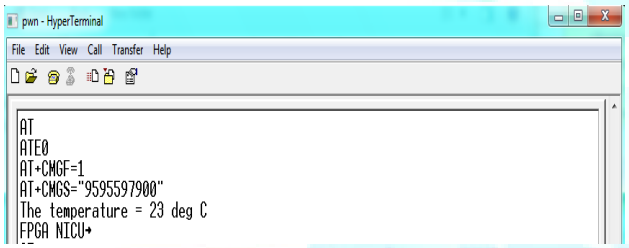

Fig. 5 The HyperTerminal Window showing AT commands sent to drive GSM SIM900A module.

5. Conclusion

The research work deals with monitoring the NICU parameters remotely. For this the Xilinx Core Generator system was used to design the MicroBlaze processor based UART soft IP core which was interfaced with a GSM module SIM900A. The GSM module was driven by sending necessary AT commands through the UART of MicroBlaze processor. The 8 bit input for this Soft IP Core implemented in Xilinx FPGA Spartan 3E is given; it is associated with the ambient temperature inside the NICU. The system sends the temperature information to the doctor's cellular phone through GSM module in the form of SMS.

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